# Analysis and Design of Analog Integrated Circuits

### Third Edition

PAUL R. GRAY
ROBERT G. MEYER
University of California, Berkeley

John Wiley & Sons, Inc.
New York · Chichester · Brisbane · Toronto · Singapore

*To Liz and Judy*

Aquisitions Editor   Steven Elliot
Marketing Manager   Susan Elbe
Production Supervisor   Elizabeth Austin
Designer   Pedro A. Noa
Manufacturing Manager   Andrea Price
Copy Editing Supervisor   Deborah Herbert
Illustration   Jaime Perea

This book was set in Times by Doyle Graphics, Ltd.
and printed and bound by Hamilton Printing.
The cover was printed by Lehigh.

Recognizing the importance of preserving what has
been written, it is a policy of John Wiley & Sons, Inc.
to have books of enduring value published in the
United States printed on acid-free paper, and we exert
our best efforts to that end.

worst case $W/L$ mismatch is 2 percent, the device thresholds are identical, $X_d = 0$, and the load resistors are identical.

3.21 For the circuit of Fig. 3.57a, determine the input offset voltage if the transistor base width mismatch by 10 percent but otherwise the circuit is balanced.

3.22 For the circuit of Fig. 3.63, determine the input offset voltage if the JFET channel widths mismatch by 10 percent but otherwise the circuit is balanced. Assume that $I_{DSS} = 1\,\text{mA}$, $V_p = -2\,\text{V}$. The bias current is much lower than $I_{DSS}$ and so the dominant offset contribution is $\Delta V_p$.

## REFERENCES

1. R. J. Widlar. "Some Circuit Design Techniques for Linear Integrated Circuits," *IEEE Transactions on Circuit Theory*, Vol. CT-12, pp. 586–590, December 1965.

2. H. R. Camenzind and A. B. Grebene. "An Outline of Design Techniques for Linear Integrated Circuits," *IEEE Journal of Solid State Circuits*, Vol. SC-4, pp. 110–122, June 1969.

3. J. Giles. *Fairchild Semiconductor Linear Integrated Circuits Applications Handbook.* Fairchild Semiconductor, 1967.

4. C. L. Searle, A. R. Boothroyd, E. J. Angelo, P. E. Grey, and D. O. Pederson. *Elementary Circuit Properties of Transistors*. Wiley, New York, 1964, Chapter 7.

5. R. D. Thornton, C. L. Searle, D. O. Pederson, R. B. Adler, and E. J. Angelo. *Multistage Transistor Circuits*. Wiley, New York, 1965, Chapter 6.

6. R. Castello and L. Tomasini. "1.5-V High-Performance S-C Filters in BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 26, pp. 930–936, July 1991.

7. R. D. Middlebrook. *Differential Amplifiers*. Wiley, New York, 1963.

8. L. J. Giacoletto. *Differential Amplifiers*. Wiley, New York, 1970.

9. J. Wallmark and H. Johnson (Eds.). *Field Effect Transistors: Physics, Technology, and Applications*. Prentice-Hall, Inc., Englewood Cliffs, N.J. 1966, Chapter 3.

10. G. Erdi. "A Low-Drift, Low-Noise Monolithic Operational Amplifier for Low Level Signal Processing." *Fairchild Semiconductor Applications Brief*, No. 136, July 1969.

11. H. C. Lin. "Comparison of Input Offset Voltage of Differential Amplifiers Using Bipolar Transistor and Field-Effect Transistors," *IEEE Journal of Solid-State Circuits*, Vol. SC-5, pp. 126–129, June 1970.

12. M. Pelgrom, A. Duinmaijer, and A. Welbers. "Matching Properties of MOS Transistors," *IEEE Journal of Solid-State Circuits*, Vol. 24, pp. 1433–1440, October 1989.

# Chapter 4

# Transistor Current Sources and Active Loads

## 4.1 Introduction

Current sources made by using active devices have come to be widely used in analog integrated circuits both as biasing elements and as load devices for amplifier stages. The use of current sources in biasing can result in superior insensitivity of circuit performance to power-supply variations and to temperature. Current sources are frequently more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the value of bias current required is small. When used as a load element in transistor amplifiers, the high incremental resistance of the current source results in high voltage gain at low power-supply voltages.

The first section of this chapter analyzes the basic types of current-source circuits that are commonly used in both bipolar and MOS technology. In the first section of this chapter, the output current and output resistance of each type are considered and the effects of device mismatches are analyzed. The second section of the chapter deals with the design of bias circuits for integrated circuits, with the objective of obtaining insensitivity of bias currents to temperature and power-supply voltage variations. Finally, the use of the transistor current source as a load element in amplifier stages is considered.

## 4.2 Current Sources

### 4.2.1 Simple Current Source

The simplest form of current source consists of a resistor and two transistors shown in Fig. 4.1 using bipolar transistors. Transistor $Q_1$ is diode connected, forcing the collector-base voltage to zero. In this mode, no injection takes place at the collector-base junction since it is at zero bias, and the transistor behaves as if it were in the forward-active region. We will neglect junction leakage currents and assume identical transistors, and assume that the output resistance of $Q_2$ is infinite. Since $Q_1$ and $Q_2$ have the same base-emitter voltage, their collector currents will be equal:

$$I_{C1} = I_{C2}$$

Summing currents at the collector of $Q_1$ yields

$$I_{ref} - I_{C1} - 2\frac{I_{C1}}{\beta_F} = 0$$

and thus

$$I_{C1} = \frac{I_{ref}}{1 + \frac{2}{\beta_F}} \approx I_{C2}$$

If $\beta_F$ is large, the collector current of $Q_2$ is nearly equal to the reference current

$$I_{C2} \cong I_{ref} \approx \frac{V_{CC} - V_{BE(on)}}{R}$$

Thus for identical devices $Q_1$ and $Q_2$, the output and reference currents are equal. Actually, the devices need not be identical; the emitter areas of $Q_1$ and
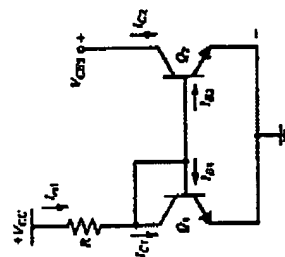


Figure 4.1   A simple two-transistor current source

can be made different, which will cause the $I_S$ values for the two transistors to be different. The two collector currents $I_{C1}$ and $I_{C2}$ will then have a constant ratio rather than being equal, as shown by (4.1). This ratio can be either less than or greater than unity, and thus any desired output current $I_{C2}$ can be derived from a fixed reference current. However, area ratios greater than about five to one consume a large die area because of the area of the larger of the two devices. Thus for the generation of large current ratios, other methods discussed in later sections, are usually preferable. Since the input current is reflected in the output, this circuit is often called a "current mirror".

One of the most important aspects of current-source performance is the variation of the current-source current with changes in voltage at the output terminal. This is characterized by the small-signal output resistance of the current source. For example, the common-mode rejection ratio of the differential amplifier depends directly on this resistance, as does the gain of the active-load circuit. We assumed, in writing (4.1), that the collector currents of the transistors are independent of their collector-emitter voltages. Actually, the collector current increases slowly with increasing collector-emitter voltage, as illustrated in Fig. 4.2. As discussed in Chapter 1, this base-width modulation effect can be represented for large-signal conditions by the expression

$$I_C = I_S \left(\exp\frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$

where $V_A$ is the Early voltage. A typical value of the Early voltage for npn transistors is 130 V. Thus, for example, if the collector-emitter voltage of $Q_1$ is held at $V_{BE(on)}$ and if the collector voltage of $Q_2$ is at 30 V, then the ratio of $I_{C2}$ to $I_{C1}$ would be

$$\frac{I_{C2}}{I_{C1}} = \frac{1 + \frac{V_{CE2}}{V_A}}{1 + \frac{V_{CE1}}{V_A}} = \frac{1 + \frac{30}{130}}{1 + \frac{0.6}{130}} \approx 1.25 \tag{4.4}$$
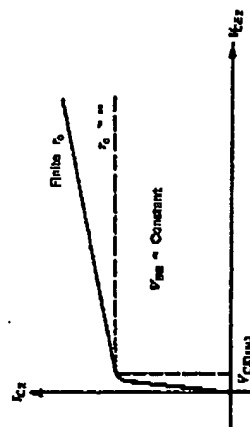


Figure 4.2   Collector characteristics for an npn transistor for the hypothetical case of $r_o = \infty$, and the actual case for which $r_o$ is finite.